

Synopsis V1.2
Single Event Latchup Testing of the
AD7664 Analog Devices Analog to Digital Converter

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I. Introduction

This study was undertaken to determine the latchup susceptibility AD7664 Analog Devices Analog to Digital Converter. The device was monitored for latchup induced high power supply currents by exposing it to a number of heavy ion beams at the Texas A&M University Cyclotron Single Event Effects Test Facility (TAMU) and the proton beam at Indiana University Cyclotron Facility (IUCF).

II. Devices Tested

The devices were manufactured by Analog Devices, Inc and all devices were characterized prior to exposure. The seventeen devices (12 at TAMU and 5 at IUCF) tested were from date code 0110.

III. Test Facilities

Facility: Texas A&M University Cyclotron Single Event Effects Test Facility

Flux: 1.2×10^1 to 1.2×10^5 particles/cm²/s.

Table I		
Ion	Energy (MeV)	LET (MeVcm²/mg)
Ar	496	8.69
Ar	385	10.0
Ar	269	12.0
Ar	155	15.0
Kr	912	29.3
Kr	523	35
Xe	1291	53.9

Facility: Indiana University Cyclotron Facility

Proton Energy: 189.9 MeV incident on DUT structure

Flux: 1.1×10^9 to 1.5×10^9 protons/cm²/s.

Temperature: room temperature

IV. Test Methods

Test Hardware:

The Test Layout for the AD7664 Latchup Experiment (See Figure 1) consists of a multi-channel power supply, a digitizing oscilloscope, Digital Multimeters (DMM's), and a function generator. Control of all test equipment was performed remotely via General Purpose Interface Bus (GPIB) with a Laptop computer as master. All relevant equipment connections to Device Under Test (DUT) board, are made using RG-58 BNC cable and scope probes. The DUT board is made up of two sections, Bias/Configuration pertaining to all devices under test and Latchup monitoring for high speed shut down and current signature capture.

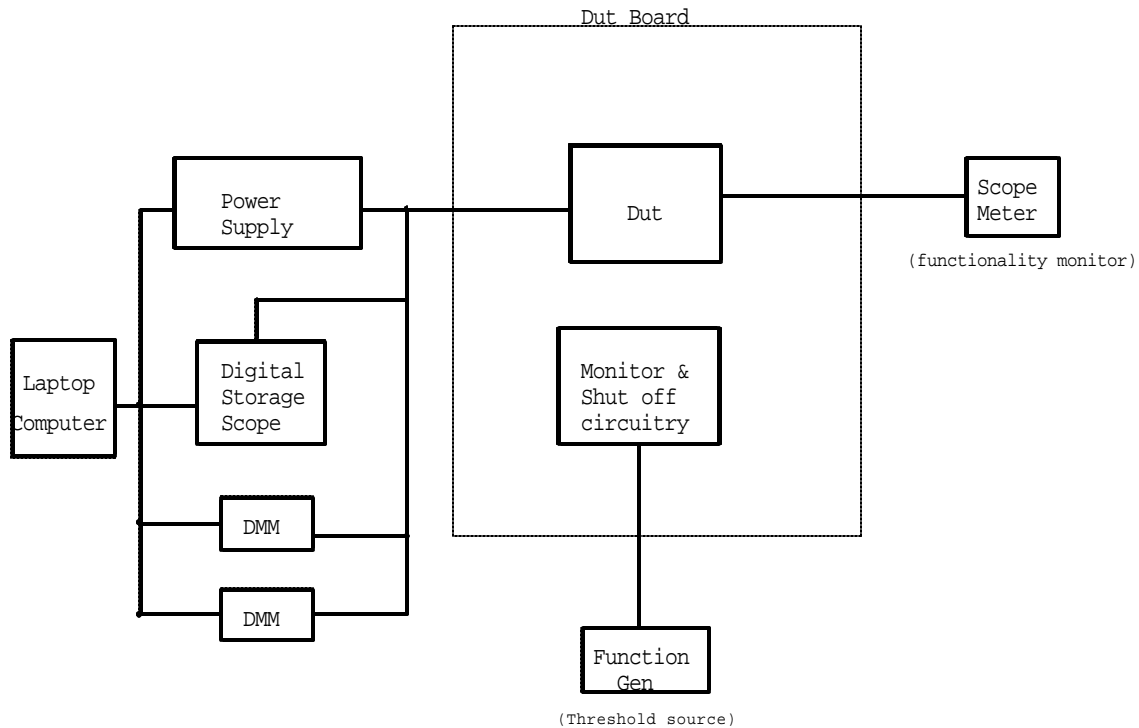


Figure 1. Block diagram for overall test setup for the AD7664.

Bias conditions for the AD7664 (See Figure 2) consisted of separate 5-volt DC supplies for Avdd and Dvdd/Ovdd. Device configuration included operating in the “Warp” mode (500khz conversion rate), parallel data interface, and straight binary mode. A conversion clock was produced by an on board 555 Timer, which provided a TTL compatible output in order to achieve the maximum conversion rate allowable. The analog source is a variable DC supply, capable of supplying the entire range of voltages from 0 to 2.5 volts. Throughout the experiment, a 1-volt DC input was applied to the converter.

The design used for monitoring nominal to latchup current conditions is shown in Figure 3. The monitoring system begins with 1 ohm shunt resistors for measuring a voltage representation of the current drawn at the Analog and Digital Power pins. Threshold and shut off circuits, utilizing difference amplifiers and voltage comparators,

were used to trigger device power shutoff once the device current exceeded a predetermined value.

The voltage drop across the 1 ohm shunt resistor is amplified by a factor of approximately 5 for Dvdd/Ovdd and 1 for Avdd in order to increase signal to noise ratio and to utilize a single threshold setting for both currents. Once the amplified shunt voltage value eclipsed the threshold level, the voltage comparator produced a signal, which via some control logic, would switch a relay that disconnected source power to both power inputs in a time period of approximately 50 microseconds.

Test points were provided for a digitizing scope and a pair of DMM's. The Digital Scope captured and saved the real time current signature during post and pre latch up conditions (sub-microsecond resolution), while the DMM's were used to record strip charts of currents (millisecond resolution) during the entire irradiation run.

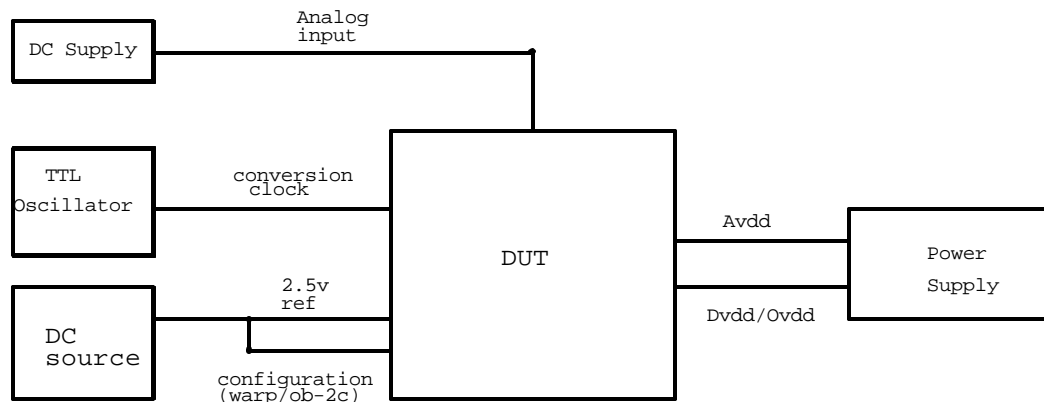


Figure 2. DUT biasing and configuration block diagram.

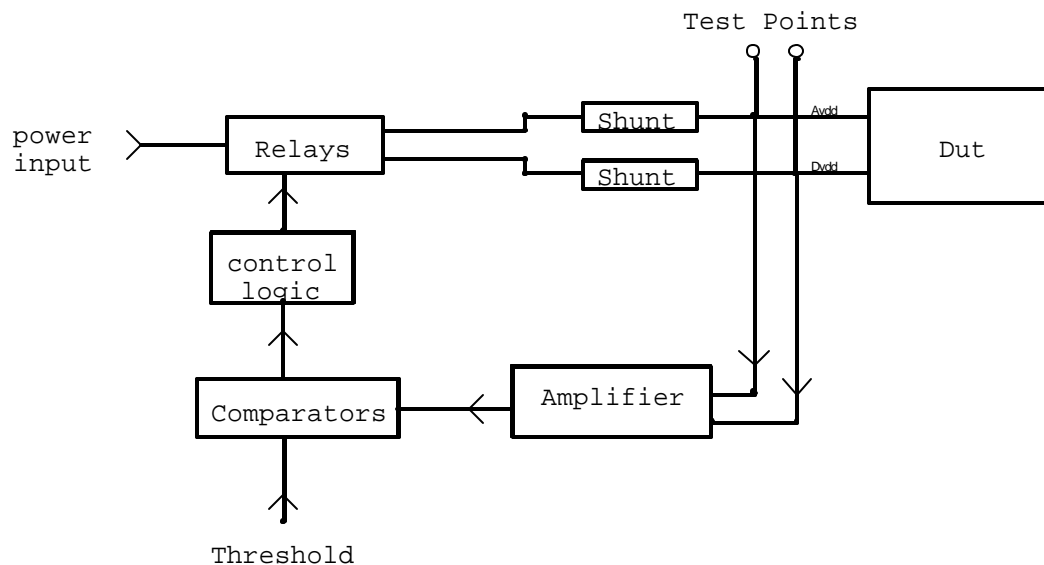


Figure 3. Latchup monitoring and protection block diagram.

Software:

Customized LABVIEW⁷ software provided a user interface to control signals to the DUT. The software also automatically monitor supply currents and generated a file history.

Test Techniques:

The AD7664 was tested for latchup in three conditions. The first of these was to accurately determine the latchup cross section as a function of Linear Energy Transfer (LET). The second condition was to measure the latchup current signature as a function of LET. Finally, five DUTs were placed in the flight configuration of the IMPACT instrument, to fly on the STEREO spacecraft, to evaluate the latchup protection system performance designed into the instrument.

In the first condition, the primary concern was measuring the number and types of latches that occur and their variation as a function of LET. To do this the DUTs need to be protected as much as possible. To this end, the thresholds for the latchup monitoring and protection setup were set to values just above nominal operating values. In this way, power was removed from the parts before any damage could occur. With these settings, the DUTs were placed into the beam and monitored for a latch condition. As soon as the latch condition was observed, the beam was stopped and the beam parameters were recorded. This process was repeated at least three times at each condition over four DUTs and all the LETs listed in Table I. In between each run, the DUT was monitored for proper performance before the next run commenced.

The second stage of the testing was to accurately measure the latchup characteristics. Specifically, determining if (1) the latches were destructive or non-destructive, (2) if non-destructive what limiting current values were achieved and (3) what are the rise-time characteristics of the latchup current signature. To do the first of these determinations, the latchup threshold levels were gradually increased to allow for the current level where the latch became destructive to be determined. During these tests, the digital scope would capture the current transient by capturing the signal every 10 ns, 50,000 times. Approximately 20% of these points were before the trigger point and the remaining 80% after, giving a transient current from 100 μ s before the trigger to approximately 400 μ s after the trigger. The DUTs were placed in the beam until the latchup current was captured and the beam turned off. This process was continued until sufficient current samples were collected across seven DUTs.

The final stage of the stage consisted of place five DUTs in their appropriate places on the engineering board of the IMPACT instrument. The instrument has a latchup protection scheme that removes power from the instrument upon detecting high current from the AD7664. The software talking to the instrument could determine when data conversion ceased and when power was removed. Each of the five devices was sequentially placed in the beam and the software monitored for latchup conditions. Upon detection of the latchup protection circuit initiation, the beam was stopped and its

parameters were recorded. This was repeated five times for each DUT at the two highest LET undegraded ion beams.

V. Heavy Ion Results

Four Analog to Digital Converters were tested to measure the latchup cross section under the above conditions. Each part was placed in the beam until a latch event occurred and then the beam fluence was recorded. This was repeated a number of times at the given LET for each of the DUTs. An average cross section was determined for a given LET as the number of latchup events observed (number of runs at that LET as every run led to a latchup event) divided by the total fluence of all the runs at that LET. This averaging method is reasonable as there was no DUT to DUT variation observed. This process was then repeated for each LET in Table I. The cross section results are presented in Figure 4. A Weibull fit to the data gives an LET threshold for latchup of approximately $7 \text{ MeV-cm}^2/\text{mg}$ and a saturation cross section is approximately $1.2 \times 10^{-3} \text{ cm}^2$.

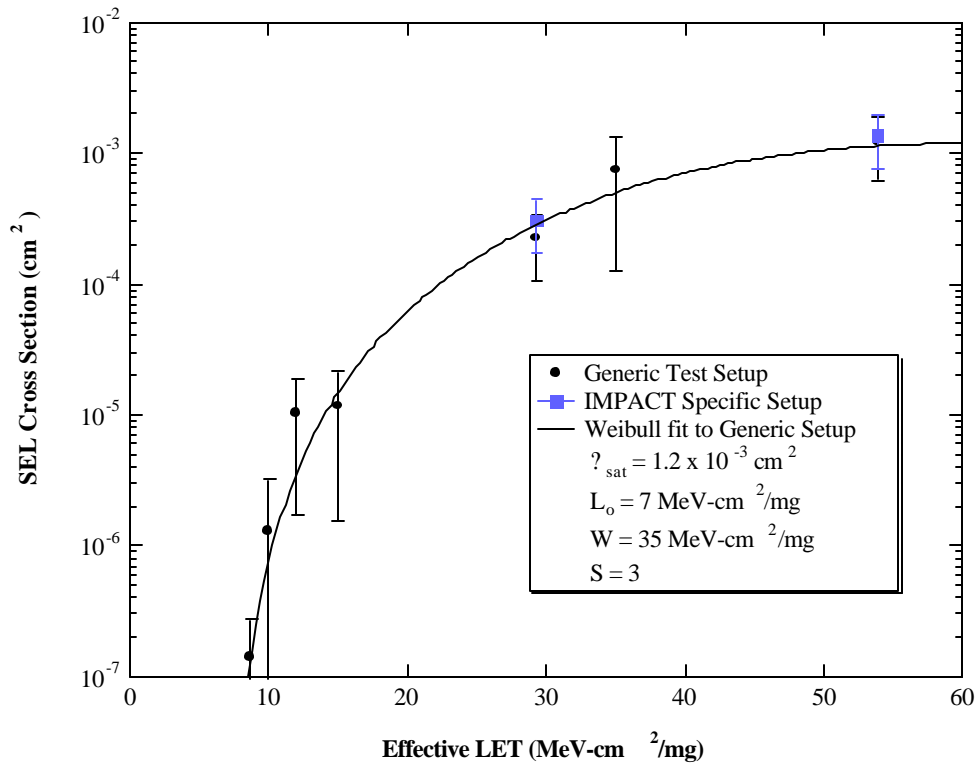


Figure 4. Latchup cross section as a function of the effective LET for the AD7664 Analog to Digital Converter. The curve shows an approximate threshold of $7 \text{ MeV-cm}^2/\text{mg}$ and a saturation cross section of greater than 10^{-3} cm^2 . The error bars represent 3 sigma deviation based on the number of observed events.

There are two objectives to the second phase of this testing. The first is to determine the nature of the latchup (i.e., destructive or non-destructive). The second is to determine the characteristics of the latchup current signature.

To address the first of these, it must be understood that as pointed out in the hardware description, three power supplies were used: One was to supply power to the analog V_{dd} , a second to supply power to the digital V_{dd} , and finally a third was used to supply power to the latchup protection circuitry and the control lines on the DUT (the control logic lines that placed the device in a given operational state). Not expecting an issue with them, the control line power supply was only hardware current limited at the power supply while the other two were current limited via a software controllable method that allowed the selection of a current limit, in addition to the hardware limit set at the power supply.

During this phase of the testing, the analog and digital supply hardware current limits were set to 2 Amps and the software limiting (via the latchup protection circuitry) was varied from the conditions used in the first phase (approximately 10 mA above nominal values) to 850 mA. The largest current observed for the digital supply was approximately 100 mA and the analog supply was approximately 700 mA. When the case was run with the trip point set to 850 mA, the current would rise to the 600 – 700 mA range and saturate, remaining on as the latchup protection circuit would not remove the power supplies.

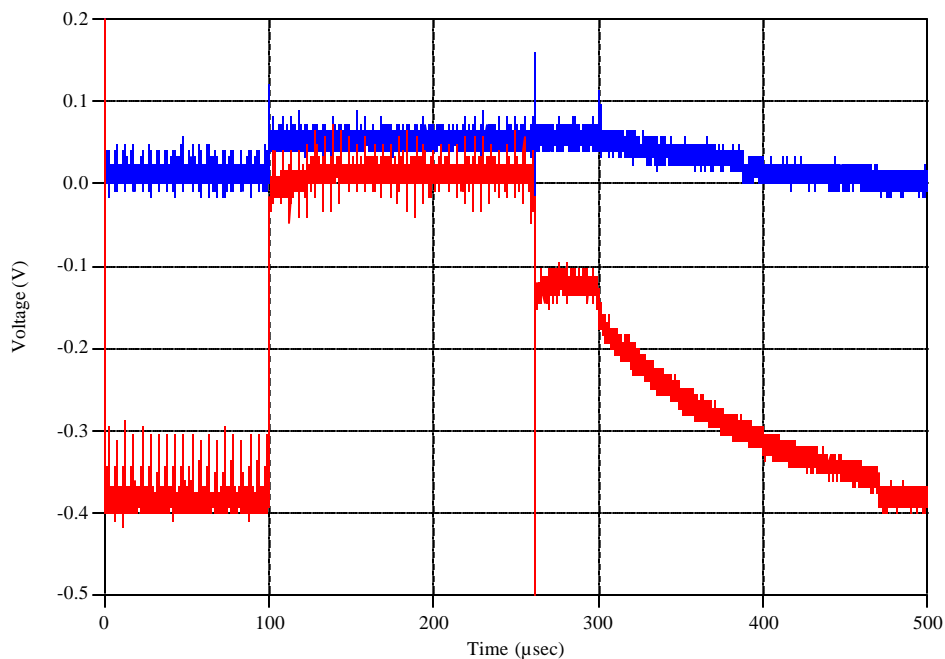


Figure 5. Sample long-time latchup signature showing the onset of latchup starting at 100 μsec and the drop out of latch, after power removal, at approximately 275 μsec. The blue curve (upper curve) is the digital current transient (voltage transient across a 1 ohm resistor) and the red curve (lower curve) is the analog current transient.

Figure 5 shows the digital and analog current transients for the condition of a 400 mA latchup protection circuit trip point. The digital curve (blue, upper) shows about a 50 mA transient and the analog current transient shows a rapidly rising current at approximately 120 μ s exceeds the 400 mA current trip point (The logic level out of the comparator is used to trigger the scope as well as the latchup protection circuit). It takes approximately 150 μ s for the latchup protection circuit to actually remove the power supply and the current begin to decrease. The “shoulder region” after the current trip has to do with the control lines and will be address later.

Figure 6 shows the same transient but only the first few microseconds are plotted. From this figure it is easy to see that there are two transient regions. The first being a very rapid rise followed then by a more slowly rising transient to the trip level. The rapid rise occurs over the course of about 200 ns and the second stage rise takes a couple of microseconds. The first stage is the rise due to the latch while the second is the current response time of the measurement circuitry. If the current limit is set to 850 mA, the rise to near the saturation current occurs over the same 200 ns. It should also be stated that Figure 5 represents the same current transient when the trip point is set below 400 mA. This comes about because of the 150 μ s delay in triggering the latchup protection circuit until the power is actually removed. During this time, the latchup current level will continue to rise but at not quite the same rate due to the latchup protection circuit being in the circuit. This lowers the maximum current observed but not to the level of the trip point. Therefore, one should assume that the actual current that will flow through the device will be substantially higher than the current trip point that may be set in a latchup protection circuit.

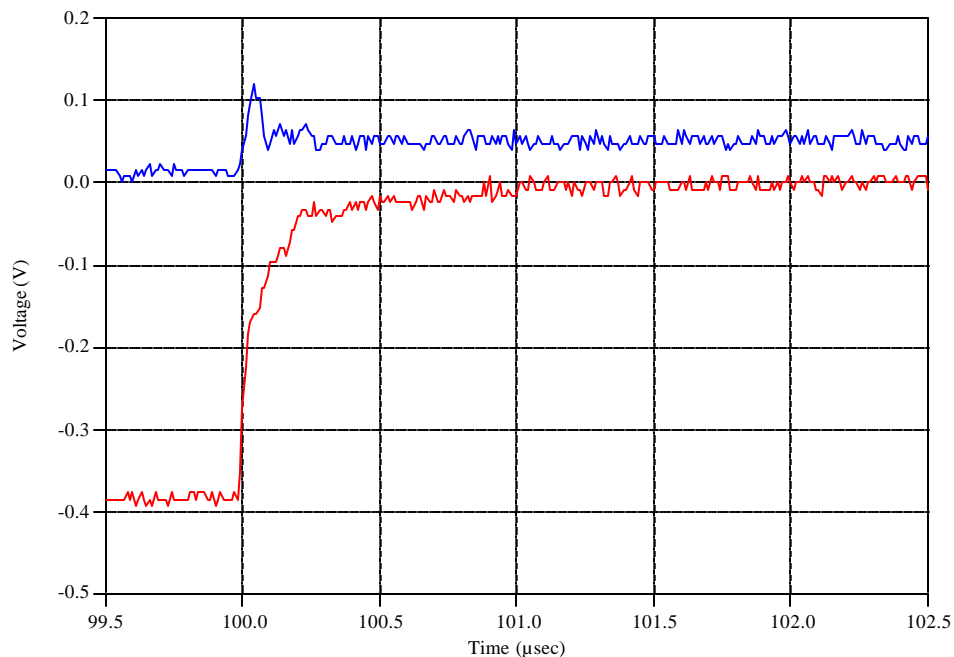


Figure 6. Sample short-time latchup signature showing the rise time to be on the order of 200 nsec.

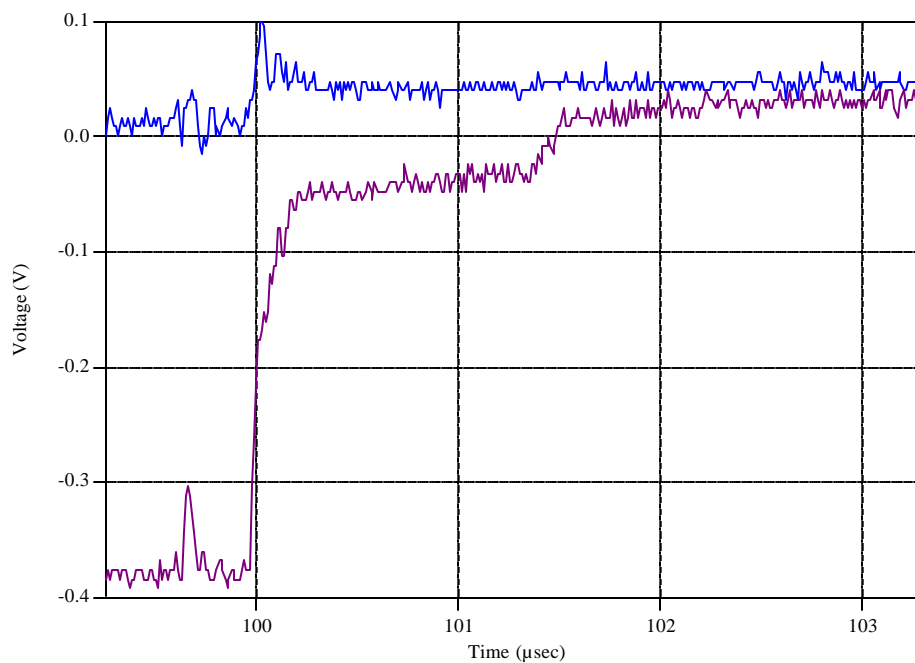


Figure 7. Latchup current signature showing a secondary latch causing the current to rise a second time. The part was non-functional after this latchup.

Figure 7 shows the beginning portion of the current transient seen when the control line hardware current limit was raised to 300 mA (and maintaining an 850 mA trip for

the analog and digital supplies). The current rises as observed previously but then a second rapid rise occurs in the analog supply line. No monitoring of the control line power was possible so it is impossible to state whether this second rise is associated with any event in that current. However, this current signature was never observed while the control line limit was set to 200 mA. Six devices were tested with the 850 mA trip on the analog and digital supplies and various current limits on the control line supply (with the smallest being 300 mA). All six devices experienced a destructive event. Therefore, the conclusion can be drawn that if the control line supply is not limited to 200 mA or below, latchup events will be destructive. Otherwise, the latchup current will rise to levels of 600 – 700 mA and the event will not be destructive (at least not immediately as there may be latent damage that will be discussed later).

With this information in mind, the “shoulder region” can now be addressed. Most likely, even in the events with the control line limit set to 200 mA, an effect in the control logic is still causing an increase in current draw from the power supply. This is seen as a sag in the voltage being supplied to the latchup protection circuit. This voltage sag could cause an impact on how well and exactly how the latchup protection circuit will work. Future testing of this device should split the control line power from the power to the latchup protection circuit to allow optimal performance of the circuit and a software controllable limit on the control line power supply.

IMPACT is an instrument that will fly on STEREO and is investigating the use of the AD7664. To this end, a latchup protection circuit is implemented in the instrument design. The final stage of the testing was to evaluate the effectiveness of the protection circuitry. To do this the devices were sequentially placed in the beam and allowed to latch. In every case where a latchup occurred, the latchup protection circuitry tripped and the power was removed from the instrument. Also in every case, when power was restored, the instrument resumed normal operations. At each protection circuit trip (as device current could not be monitored within the instrument) the beam was stopped and the fluence recorded. In the same manner as the first stage of the testing, described above, a cross section was calculated for the two LET points run. These are also plotted in Figure 4 as blue squares. The agreement with the stage one data points and the Weibull fit is very good. It should also be noted that the power to the control lines was limited to less than 10 mA and therefore no destructive events were expected.

VI. Proton Results

Five samples were exposed to protons while looking for latchup. All five samples were taken to total dose failure (approximately 21 krad of protons) in incremental steps. Only one latchup event was observed during all exposures of all five parts. The total exposure for the five parts was approximately 2×10^{12} protons/cm². This yields a cross section of approximately 5×10^{-13} cm². The one observed latchup event was non-destructive.

VII. Summary

Considering the cross section data in Figure 4, the AD7664 Analog Devices Analog to Digital Converter is considered to have an LET threshold for latchup of approximately 7 MeV-cm²/mg. If the power supply providing the control lines is current limited to 200 mA or less, all observed latchups were non-destructive. However, if the control line power is not limited, latchup events will be destructive. For both types of latchup events, the saturation cross section is approximately 1.2×10^{-3} cm². Future testing of this device should split the control line power from the power to the latchup protection circuit to allow optimal performance of the circuit and a software controllable limit on the control line power supply.

Proton sensitivity was also tested. One latchup event was seen indicating proton sensitivity but the total fluence was very high yielding a low cross section for the event. The cross section was approximately 5×10^{-13} cm².

In addition to proton effect, the effect of latent damage is also a possibility. Latent damage is an effect where a device that does not destructively latch can still have significant damage that will impact the device reliability (e.g., shortened lifetime). This testing demonstrated both destructive and non-destructive latchup modes but no attempt was made to investigate latent damage. This investigation is highly recommended prior use in flight.

VIII. Recommendations

In general, devices are categorized based on heavy ion test data into one of the four following categories:

Category 1 – Recommended for usage in all NASA/GSFC spaceflight applications.

Category 2 – Recommended for usage in NASA/GSFC spaceflight applications, but may require mitigation techniques.

Category 3 – Recommended for usage in some NASA/GSFC spaceflight applications, but requires extensive mitigation techniques or hard failure recovery mode.

Category 4 – Not recommended for usage in any NASA/GSFC spaceflight applications.

The AD7664 Analog Devices Analog to Digital Converters are Category 3 devices. If latent damage is demonstrated, this part would then be considered a Category 4 device.